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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/943,238	10/03/1997	MASAAKI HIROKI	0756-1724	9123

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/943,233	MASAAKI HIROKI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-110* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *41-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *see O/A* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed April 11, 2002 has been entered. Therefore claims 41 to 110 are currently pending in the application. Claims 21 to 40 have been cancelled by the amendment.

Information Disclosure Statement

The IDS filed on 11/26/99,1/10/00, 2/14/00, 10/05/00,1/12/01,6/5/01, 12/13/00, 7/6/01, 11/13/01 and 4/30/02 have been considered and contract employees instructed to enclose a copy of the initialed 1449s along with this Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41 to 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,960, 710, herein after Tanaka) and Aoyama (Jp No. 62-283664, herein after Aoyama) and Shindo et al. (U.S. Patent No. 5,181, 132, herein after Shindo).

With respect to claim 41, Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23),

depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion. (figs. 8 c, d).

With respect to claim 42, wherein a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

Tanaka does not specifically describe its CVD as being carried out in the presence of a mixture gas containing a silane, phosphine and hydrogen.

However, Aoyama, a patent from the same filed of endeavor, describes in its abstract lines10 and 18, depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen to form thin silicon epitaxial layers that are grown with abrupt doping profile and to carry out the reaction at lower temperatures that is possible by the introduction of hydrogen.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Aoyama's mixture gas containing a silane, phosphine and hydrogen in Tanaka's process steps to form thin silicon epitaxial layers that are grown with abrupt doping profile and to carry out the reaction at lower temperatures that is possible by the introduction of hydrogen.

With respect to claim 43, further including a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel (Tanaka fig. 8 d # 28).

With respect to claim 44, wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

Tanaka and Ayomo do not specifically disclose the gate electrode as a doped silicon film and a molybdenum film formed thereon.

However, Shindo, a patent from the same filed of endeavor, describes in col. 8 lines 45-47 describes a multi layer gate electrode including doped silicon film having a molybdenum film formed thereon to form gate electrodes with good bonding strength and is appropriate for forming a sub-micron pattern.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include the gate electrode including doped silicon film having a molybdenum film formed thereon to form gate electrodes with good bonding strength and is appropriate for forming a sub-micron pattern.

With respect to claim 45 wherein said gate electrode comprises aluminum. (Shindo col. 6 lines 20-25).

With respect to claim 46 wherein said gate insulating comprises silicon oxide (Tanaka col. 1 lines 64-66).

With respect to claim 47 wherein amorphous semiconductor film is deposited through CVD. (Tanaka col. 5 lines 13-15).

With respect to claim 48, wherein amorphous semiconductor film is deposited to a thickness of 500 to 5000 A^0. (Shindo col. 11 lines 35-45 and Tanaka col. 5 lines 23-27).

With respect to claim 49, wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film (Tanaka fig. 8 c).

With respect to claim 50, wherein the pixel electrode extends over said channel region (Tanaka fig. 8 d).

With respect to claim 51, Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a color filter over a second substrate (Shindo fig. 12 # 13 col. 10 lines 57), forming a second organic leveling film

over the color filter (Shindo fig. 12 # 15) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other herein said opening has a tapered configuration so that a electrode diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion. (figs. 8 c, d).

Claims 52 to 60 repeat the steps of claims 41-50 and therefore are rejected for reasons set out above.

Claims 61 Tanaka describes a method of manufacturing an active matrix type display device including the steps of :

Forming a gate electrode over an insulating surface of a substrate. (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a resin black matrix over a second substrate (Shindo col. 1 lines 48-51), forming a second organic leveling film over the color filter (Shindo fig. 12 # 15) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter

electrode and said pixel electrode are opposed to each other herein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion. (figs. 8 c,d).

Claims 62 to 70 repeat the steps of claims 51 to 60 and are rejected for the same reasons set out above.

Claims 71 Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate. (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a color filter over a second substrate (Shindo fig. 12 # 13 col. 10 lines 57), forming a second organic leveling film over the color filter (Shindo fig. 12 # 15) forming a resin black matrix over said substrate (Shindo col. 1 lines 48-51) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other herein said opening has a tapered

configuration so that a diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion (figs. 8 c,d).

Claims 72 to 80 repeat the steps of claims 51 to 60 and are rejected for the same reasons set out above.

With respect to Claims 81 Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate. (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a color filter over a second substrate (Shindo fig. 12 # 13 col. 10 lines 57), forming a second organic leveling film over the color filter (Shindo fig. 12 # 15) forming a resin black matrix over said substrate (Shindo col. 1 lines 48-51) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other herein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower

portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion (figs. 8 c,d).

Claims 82 to 90 repeat the steps of claims 51 to 60 and are rejected for the same reasons set out above.

With respect to Claim 91 Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate. (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a color filter over a second substrate (Shindo fig. 12 # 13 col. 10 lines 57), forming a second organic leveling film over the color filter (Shindo fig. 12 # 15) forming a resin black matrix over said substrate (Shindo col. 1 lines 48-51) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other herein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a

first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion (figs. 8 c,d).

Claims 92 to 100 repeat the steps of claims 51 to 60 and are rejected for the same reasons set out above.

With respect to Claims 101 Tanaka describes a method of manufacturing an active matrix type display device including the steps of:

Forming a gate electrode over an insulating surface of a substrate (Tanaka fig. 8 a # 22), forming a gate insulating film over the gate electrode (Tanaka fig. 8 a # 23), depositing an amorphous silicon semiconductor film on gate insulating film (fig. 8 a # 24), patterning said semiconductor film into an island comprising a channel region (figs. 8 b and c), forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface (fig. 8 c # 26), forming an opening in said organic leveling film (fig. 8 c) and forming a pixel electrode over said organic leveling film through the opening (fig. 8 c # 27), forming a color filter over a second substrate (Shindo fig. 12 # 13 col. 10 lines 57), forming a second organic leveling film over the color filter (Shindo fig. 12 # 15) forming a resin black matrix over said substrate (Shindo col. 1 lines 48-51) forming a counter electrode on second leveling film and facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other herein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion (fig. 8 c to d), and wherein said upper portion of said opening is rounded from a

first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion (figs. 8 c,d).

Claims 102 to 110 repeat the steps of claims 51 to 60 and are rejected for the same reasons set out above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

January 21, 2003.